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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,222	08/18/2003	Kenji Yoshida	241677US2	2212
22850	7590	05/17/2006	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			STEVENS ON, ANDRE C	
			ART UNIT	PAPER NUMBER
			2812	

DATE MAILED: 05/17/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/642,222	Applicant(s) YOSHIDA ET AL.	
	Examiner Andre' C. Stevenson	Art Unit 2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 29 March 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) 11-20 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2 and 7-10 is/are rejected.
- 7) ☒ Claim(s) 3-6 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 18 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>02/17/05, 01/12/04</u> . | 6) <input type="checkbox"/> Other: _____ |

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Detailed Action

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Election/Restrictions

Applicant's election **without traverse** of Group I, claims 1-10, in the reply filed on March 29, 2006 is acknowledged.

Claims #11 through 20 have been withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without traverse** in the reply filed on November 02, 2005.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on 02/17/05 and 01/12/04 were filed before the first action on the merits. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims #1, 2 and 7 through 10 are rejected under 35 U.S.C. 102(e) as being anticipated by Satoh et al. (U.S. Pat. No.6,946,723, Pat. Date 09/20/05, Filed 03/16/01).

Satoh substantially shows the claimed invention, as shown in figures 1-44 and corresponding text, in a device and manufacturing method comprising, **pertaining to claim #1**, a testing method for a semiconductor device, having wirings composed of copper or an alloy mainly composed of copper, comprising (**column #9, lines 6-21**): executing an acceleration test for eliminating an initial failure of the wirings due to stress migration (**column #9, lines 60-67; column #10, lines 1-4**); and checking whether or not the wirings are broken (**column #36, lines 35-48**). *Pertaining to claim #2*, Satoh shows, a system further comprising: stress sensing means for sensing a voltage stress imposed on the gate oxide film of each said device while the wafer is being exposed to the electromagnetic wave that has been generated by the electromagnetic wave generating means; and control means for controlling the intensity of the electric field, which is represented by the electromagnetic wave generated by the electromagnetic wave generating means, so that the voltage stress sensed by the stress sensing means falls within a preset threshold value range (**column #9, lines 60-67; column #10, lines 1-4**). *Pertaining to claim #7*, Satoh shows, a testing method wherein executing the acceleration test comprises increasing and decreasing the temperature of the semiconductor device at least once in a second temperature zone covering $\pm 40^{\circ}\text{C}$ of a reference temperature set

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(column #9, lines 60-67; column #10, lines 1-4). Pertaining to claim #8, Satoh shows, a testing method wherein executing the acceleration test comprises increasing and decreasing the temperature of the semiconductor device in the second temperature (column #8, lines 49-60; column #9, lines 26-46). *Pertaining to claim #9*, Satoh shows, a testing method wherein executing the acceleration test comprises increasing and decreasing the temperature of the semiconductor device in the second temperature zone from 0.4 hour to two hours (column #8, lines 49-60; column #9, lines 26-46). Pertaining to claim #10, Satoh shows, a testing method wherein after semiconductor elements composing the semiconductor device are formed on a semiconductor substrate, executing the acceleration test when the wirings are formed in wiring layers through interlayer insulation films and the semiconductor elements are connected to each other via the wirings (column #1, lines 29-63; column #9, lines 6-21; column #9, lines 60-67; column #10, lines 1-4; column #36, lines 35-48; column #34, lines 20-37 and lines 48-60).

Allowable Subject Matter

Claims #3 through 6 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, depending on further search.

Claim #3

- ✓ Migration is most accelerated is a test temperature when an acceleration factor AF is maximized.

Claim #4

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- ✓ acceleration factor AF has a relationship shown by following expression;

$$AF = \{C(TO - Ta)^{-n} \cdot \exp(Ea/kTa)\} / \{C(TO - Tatest)^{-n} \cdot \exp(Ea/kTatest)\}$$

Claim #5

- ✓ The first temperature zone for at least 0.4 hour.

Claim #6

- ✓ Migration the first temperature zone from 0.4 hour to two hours.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andre' Stevenson whose telephone number is (571) 272 1683. The examiner can normally be reached on Monday through Friday from 7:30 am to 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt, can be reached on (571) 272 1873. The fax phone number for the organization where this application or proceeding is assigned is (703) 308 7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308 0956. Also, the proceeding numbers can be used to fax information through the Right Fax system;

(703) 872-9306

Andre' Stevenson

05/15/06


MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER